PATENT APPLICATION SERIAL NO. 09/080774

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/22/1998 HBORDON 00000048 122475 09080774
02 FC:101 790.00 OP
03 FC:102 82.00 OP
04 FC:103 2.00 CH 372.00 OP

PTO-1556
(5/87)

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/080,774	05/18/98	327	2816	233/248

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CONTINUING DOMESTIC DATA********
VERIFIED none
JZ

371 (NAT'L STAGE) DATA********
VERIFIED none
JZ

FOREIGN APPLICATIONS********
VERIFIED none
JZ

FOREIGN FILING LICENSE GRANTED 06/03/98

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐yes ☒no ☐yes ☒no ☐Met after Allowance Verified and Acknowledged JZ Examiner's Initials Initials	CA	9	37	4

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TITLE

OFFLINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	
$1,246		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Bib Data Sheet

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

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** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
06/03/1998

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☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Signature _____ Initials	CA	9	37	4

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FILING FEE RECEIVED		
1246	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

SPECIFICATION

TITLE OF THE INVENTION

OFFLINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER

BACKGROUND

Field Of The Invention

The field of the present invention pertains to the field of power supplies and among other things to the regulation of power supplies.

Background Of The Invention

Power supplies that convert an AC mains voltage to a DC voltage for use by integrated electronic devices, amongst other devices, are known. The power supplies are required to maintain the output voltage, current or power within a regulated range for efficient and safe operation of the electronic device. Switches that operate according a pulse width modulated control to maintain the output voltage, current, or power of the power supply within a regulated range are also known. These switches utilize an oscillator and related circuitry to vary the switching frequency of operation of the switch, and therefore regulated the power, current or voltage that is supplied by the power supply.

A problem with utilizing pulse width modulated switches is that they operate at a relatively high frequency compared to the frequency of the AC mains voltage, which results in a high frequency signal being generated by the power supply. This high frequency signal is injected back into the AC mains input and becomes a component of the AC mains signal. The

high frequency signals are also radiated by the power supply as electromagnetic waves. These high frequency signals add to the Electromagnetic Interference (EMI) of the power supply, and in fact are the largest contributors to the EMI of the power supply. The EMI generated by the power supply can cause problems for communications devices in the vicinity of the power supply and the high frequency signal which becomes a component of the AC mains signal will be provided to other devices in the power grid which also causes noise problems for those devices. Further, the radiated EMI by the power supply can interfere with radio and television transmissions that are transmitted over the air by various entities.

To combat the problem of EMI, several specifications have been developed by the Federal Communications Commission (FCC) in the United States and the European Community (EC) have established specification that specify the maximum amount of EMI that can be produced by classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing a power supply is minimizing the EMI provided by the power supply to levels with the acceptable limits of the various standards. Since, a power supply can be utilized in many different countries of the world, the EMI produced should be within the most stringent limits worldwide to allow for maximum utilization of the power supply.

A known way of minimizing the EMI provided by the power supply is by adding an EMI filter to the input of the power supply. An EMI filter generally utilizes at least one inductor, capacitor and resistor in combination. However, the greater EMI produced by the power supply the larger the components that are utilized as part of the EMI filter. The cost of the EMI filter is in large part determined by the size of the inductor and capacitor utilized. The longer the

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components, the higher the cost of the power supply. Further, simply utilizing an EMI filter does not address the radiated EMI.

Another problem associated with pulse width modulated switches results from operation of the power supply at start up. At start up, the voltage, current and power at the output of the power supply will essentially be zero. The pulse width modulated switch will then conduct for the maximum possible amount of time in each cycle of operation. The result of this is a maximum inrush current into the power supply. The maximum inrush current is greater than the current that is utilized during normal operation of the power supply. The maximum inrush current stresses the components of power supply and switch. Stress is specifically a problem for the switch, or transistor, the transformer of the power supply, and the secondary side components of the power supply. The stress caused by the maximum inrush current decreases the overall life of the power supply and increases the cost of the power supply because the maximum rating of the components used in the power supply to not destruct from the inrush currents will be greater than the maximum rating required for normal operation.

Further, when the pulse width modulated switch conducts for the maximum possible amount of time in each cycle of operation the voltage, current and power at the output of the power supply rise rapidly. Since the feedback circuit of the power supply often does not respond as fast as the operating frequency of the switch, the rapid rise of the voltage, current and power will often result in an overshoot of the maximum voltage in the regulation range which will cause damage to the device being supplied power by the power supply.

Referring to Fig. 1 a known power supply that attempts to minimize EMI and reduce startup stress is depicted. A rectifier 10 rectifies the filtered AC mains voltage 5, from EMI filter 120, input by the AC mains to generate a rectified voltage 15. Power supply capacitor 20 then

generates a substantially DC voltage with a ripple component. The rectified voltage 15 with ripple component is provided to the primary winding 35 of transformer 40 that is used to provide power to secondary winding 45. The output of secondary winding 45 is provided to secondary rectifier 50 and secondary capacitor 55 that provide a secondary DC voltage 60 at the power supply output 65 to the device that is coupled to the power supply.

In order to maintain the secondary DC voltage within a regulate range a feedback loop including an optocoupler 70, zener diode 75 and a feedback resistor 80 provides a signal indicative of the voltage at the power supply output 65 to feedback pin 85 of pulse width modulated switch 90. The voltage magnitude at the feedback terminal is utilized to vary the duty cycle of a switch coupled between the drain terminal 95 and common terminal 100 of the pulse width modulated switch 90. By varying the duty cycle of the switch the average current flowing through the primary winding and therefore the energy stored by the transformer 40 which in turn controls the power supplied to the power supply output 65 is kept within the regulated range. A compensation circuit 105 is coupled to the feedback pin 85 in order to lower the bandwidth of the frequency of operation of the pulse width modulator.

Inrush currents are minimized at start up by use of soft start capacitor 110. Soft start functionality is termed to be a functionality that reduces the inrush currents at start up. At this instant a current begins to flow through feedback resistor 80 and thereby into soft start capacitor 110. As the voltage of soft start capacitor 110 increases slowly, current will flow through light emitting diode 115 of optocoupler 70 thereby controlling the duty cycle of the switch. Once the voltage of the soft start capacitor 110 reaches the reverse breakdown voltage of zener diode 75 current will flow through zener diode 75. The approach described above will reduce the inrush currents into the power supply, however, it will be several cycles before the light emitting diode

115 will begin conducting. During the several cycles the maximum inrush current will still flow through the primary winding and other secondary side components. During these cycles the transformer may saturate, and therefore the transformer may have to be designed utilizing a higher core size than would be required for normal operation even with the use of soft start capacitor as in Fig. 1.

To reduce the EMI output by the power supply an EMI filter 120 is utilized. Additionally, pulse width modulated switch 90 is equipped with frequency oscillation terminals 125 and 130. Frequency oscillation terminal 125 and 130 receive a jitter current 135 that varies according to the ripple component of substantially DC voltage 15. The jitter current 135 is used to vary the frequency of the saw-toothed waveform generated by the oscillator contained in the pulse width modulated switch 90. The saw toothed waveform generated by the oscillator is compared to the feedback provided at the feedback pin 85. As the frequency of the saw toothed waveform varies, so will the switching frequency of the switch coupled between the drain and common terminal. This allows the switching frequency of the switch to be spread over a larger bandwidth, which minimizes the peak value of the EMI generated by the power supply at each frequency. By reducing the EMI the ability to comply with government standards is increased, because the government standards specify quasi-peak and average values at given frequency levels. Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter.

A problem associated with the EMI reduction scheme described with respect to Fig. 1 is that the ripple component will have variances due to variations in the line voltage and output load. Additionally, since the ripple may vary, design and the component value of EMI resistor

140 is difficult to determine and correspondingly design of the power supply becomes problematic.

SUMMARY OF THE INVENTION

In one embodiment the present invention comprises a pulse width modulated switch comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated circuit further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

Another embodiment of the present invention comprises a pulse width modulated switch comprising a switch comprising a control input, the switch allowing a signal to be transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state, a drive circuit that provides the drive signal, and a soft start circuit that provides a signal instructing said drive circuit to disable the drive signal during at least a portion of said on-state of the maximum duty cycle.

In an alternate embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second

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terminal according to a drive signal, a drive circuit that provides the drive signal and a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal.

In yet another embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a frequency variation circuit that provides a frequency variation signal, and a drive circuit that provides a drive signal for a maximum time period of a time duration cycle. The time duration of the cycle varies according to the frequency variation signal.

In the above referenced embodiments the pulse width modulated switch or regulation circuit may comprise a monolithic device.

An object of an aspect of the present invention is directed to a pulse width modulated switch that has integrated soft start capabilities.

Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities.

Yet another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities and integrated soft start capabilities.

A further object of an aspect of the present invention is directed toward a low cost regulated power supply that has both soft start and frequency variation capabilities.

This and other objects and aspects of the present inventions are taught, depicted and described in the drawings and the description of the invention contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a known power supply utilizing a pulse width modulated switch, and external soft start, and frequency jitter functionality.

Fig. 2 is a presently preferred power supply utilizing an pulse width modulated switch according to the present invention.

Fig. 3 is a presently preferred pulse width modulated switch according to the present invention.

Fig. 4 is a timing diagram of the soft start operation of the presently preferred pulse width modulated switch according to the present invention.

Fig. 5 is a timing diagram of the frequency jitter operation of the presently preferred pulse width modulated switch according to the present invention.

Fig. 6 is an alternate presently preferred pulse width modulated switch according to the present invention.

Fig. 7 is a timing diagram of the operation of the alternate presently preferred pulse width modulated switch of Fig. 6 according to the present invention.

Fig. 8 is a presently preferred power supply utilizing a regulation circuit according to the present invention.

Fig. 9 is a presently preferred regulation circuit according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 2, EMI filter 200 is coupled to an AC mains voltage 205. The AC mains voltage 205 is rectified by rectifier 210. The rectified voltage 215 is provided to power supply capacitor 220 which provides a substantially DC voltage 225. The substantially DC

voltage 225 is provided to the primary winding 230 of transformer 235 which stores the energy provided to the primary winding 230. When the primary winding 230 is no longer receiving energy, energy is delivered by the transformer 235 to the secondary winding 240. The voltage induced across the secondary winding 240 is rectified by rectifier 245 and then transformed into secondary substantially DC voltage 265 by secondary capacitor 260 and provided to the power supply output 267.

Energy is no longer provided to the primary winding 230 when the pulse width modulated switch 262, which is coupled to the primary winding 230, ceases conduction. Pulse width modulated switch 262 is a switch that is controlled by a pulse width modulated signal. Pulse width modulated switch 262 conducts and ceases conduction according to a duty cycle, that is in part determined by feedback from the power supply output 267. Pulse width modulated switch 262 is a switch that operates according to pulse width modulated control. Feedback to the pulse width modulated switch 262 is accomplished by utilization of feedback circuit 270, which is presently preferred to comprise a zener diode 275 in series with a resistor 280 and optocoupler 285. Optocoupler 285 provides a feedback current 290 to feedback terminal 295 of pulse width modulated switch 262. The feedback current is utilized to vary the duty cycle of a switch coupled between the first terminal 300 and second terminal 305 and thus regulate the output voltage, current or power of the power supply.

Although, it is presently preferred that the output voltage is utilized for feedback, the present invention is also capable of utilizing either the current or power at the power supply output 267 without departing from the spirit and scope of the present invention.

A portion of the current supplied at the feedback terminal 295 is utilized to supply bias power for operation of the pulse width modulated switch 262. The remainder of the current

input at the feedback terminal 295 is utilized to control the duty cycle of the pulse width modulated switch 262, with the duty cycle being inversely proportional to the feedback current.

A bias winding 310 is utilized to bias optocoupler 285 so that a feedback current can flow when light emitting diode 315 of optocoupler 285 conducts. The power supplied by the bias winding 310 is also used to charge pulse width modulation capacitor 330, the energy from which is utilized to power the pulse width modulated switch 262.

Overvoltage protection circuit 335 is utilized to prevent overvoltages from propagating through to the transformer 235.

Pulse width modulated switch 262 is supplied power during start up of the power supply by current flowing into the first terminal 300. An embodiment of one type of apparatus and method for designing a configuration for providing power to pulse width modulated switch through first terminal 300 is disclosed in commonly owned U.S. Patent No. 5,014,178 which is incorporated herein by reference in its entirety.

The drain terminal 300, source terminal 305 and feedback terminal 295 are the electrical input and/or output points of the pulse width modulated switch 262. They need not be part of a monolithic device or integrated circuit, unless the pulse width modulated switch 262 is implemented utilizing a monolithic device or integrated circuit.

Pulse width modulated switch 262 also may have soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of pulse width modulated switch 262. The power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten

(10) milliseconds. Once soft start operation is completed, pulse width modulated switch 262 operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, pulse width modulated switch 262 may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch 262 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of Fig. 1 in that the frequency range of the presently preferred pulse width modulated switch 262 is known and fixed, and is not subject to the line voltage or load magnitude variations. At low powers, those less than approximately ten (10) watts, the common mode choke which is often utilized as part of the EMI filter 120 can be replaced with inductors or resistors.

As can be seen when comparing the power supply of Fig. 1 to that of Fig. 2 the number of components utilized is reduced. This reduces the overall cost of the power supply as well as reducing its size.

Referring to Fig. 3, frequency variation signal 400 is utilized by the pulse width modulated switch 262 to vary its switching frequency within a frequency range. The frequency variation signal 400 is provided by frequency variation circuit 405, which preferably comprises an oscillator that operates at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular waveform that preferrably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal 400 is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal.

The frequency variation signal 400 is provided to soft start circuit 410. During operation soft start circuit 410 is also provided with pulse width modulation frequency signal 415 and power up signal 420. Soft start enable signal 421 goes high at power up and remains high until oscillator signal 400 reaches its peak value for the first time. Soft start circuit 410 will provide a signal to or-gate 425 to reset latch 430 thereby deactivating conduction by the switch 435, which is presently preferred to be a MOSFET. Soft start circuit 410 will instruct switch 435 to cease conduction when the soft start enable signal 421 is provided and the magnitude of the frequency variation signal 400 is less than the magnitude of pulse width modulation signal 415. In other words, start up circuit 410 will allow the switch 435 to conduct as long as soft start enable signal is high and the magnitude of the pulse width modulation signal 415 is below the magnitude of frequency variation signal 400 as depicted in Fig. 4. In this way, the inrush current at startup will be limited for all cycles of operation, including the first cycle. By limiting the inrush current during all cycles of startup operation, the maximum current through each of the components of the power supply is reduced and the maximum current rating of each component can be decreased. The reduction in the ratings of the components reduces the cost of the power supply. Soft start signal 440 will no longer be provided by the frequency variation circuit 405 when the frequency variation signal 400 reaches its peak magnitude.

Operation of soft start circuit 410 will now be explained. Soft start circuit 410 comprises a soft start latch 450 that at its set input receives the power up signal 420 and its reset input receives the soft start signal 440. Soft start enable signal 421 is provided to one input of soft start and-gate 455 while the other input of soft start and-gate 455 is provided with an output from soft start comparator 460. The output of soft start comparator 460 will be high when the

magnitude of frequency variation signal 400 is less than the magnitude of pulse width modulation oscillation signal 415.

The pulse width modulated switch 262 depicted in Fig. 3 also has frequency jitter functionality to help reduce the EMI generated by the power supply and pulse width modulated switch 262. Operation of the frequency jitter functionality will now be explained. Main oscillator 465 has a current source 470 that is mirrored by mirror current source 475. Main oscillator drive current 615 is provided to the current source input 485 of PWM oscillator 480. The magnitude of the current input into current source input 485 of PWM oscillator 480 determines the frequency of the pulse width modulation oscillation signal 415 which is provided by PWM oscillator 480. In order to vary the frequency of pulse width modulation oscillation signal 415, an additional current source 495 is provided within main oscillator 465. The additional current source 495 is mirrored by additional current source mirror 500. The current provided by additional current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases so does the voltage at the source of main oscillator transistor 505, due to the increasing voltage at the gate of main oscillation transistor and the relatively constant voltage drop between the gate and source of the main oscillation transistor 505. As the voltage at the source of main oscillation transistor 505 increases so does the current flowing through the main oscillation resistor 510. The current flowing through main oscillation resistor 510 is the same as the current flowing through additional current source 495 which is mirrored by additional current source mirror 500. Since, the presently preferred frequency variation signal 400 is a triangular waveform having a fixed period, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency

variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency would linearly rise to a peak and then immediately fall to is lowest value. In this way, the current provided to current source input 485 of PWM oscillator 480 is varied in a known fixed range that allows for easy and accurate frequency spread of the high frequency current generated by the pulse width modulated switch. Further, the variance of the frequency is determined by the magnitude of the current provided by additional current source mirror 500, which is in turn a function of the resistance of main oscillation resistor 510.

Frequency variation circuit 405 includes a current source 525 that produces a fixed magnitude current 530 that determines the magnitude of the frequency of the frequency variation signal 400. Although, the presently preferred current 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current, if a variable current is generated the frequency spread would not be fixed in time but would vary with the magnitude of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirrored by second transistor 540 and fed into third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of frequency variation circuit capacitor 550. Frequency variation circuit capacitor 550 is presently preferred to have a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of the pulse width modulated switch 262. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 560. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage 552 which is presently preferred to be four point five (4.5) volts. The output of lower limit comparator 560 will be high when the magnitude of frequency variation signal 400 exceeds lower threshold voltage 557 which is presently preferred to be one point five volts (1.5) volts. The output of

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upper limit comparator 555 is provided to the frequency variation circuit inverter 565 the output of which is provided to the reset input of frequency variation circuit latch 570. The set input of frequency variation circuit latch 570 receives the output of lower limit comparator 560. In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between upper threshold 552, 4.5 volts, and the lower threshold 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation signal 400 exceeds upper level threshold 552. This means that the reset input will receive a high signal until the magnitude of the frequency variation signal 400 rises above the upper threshold signal 552.

The charge signal 575 output by frequency variation circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal 552. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 585 and 595 current can flow into frequency variation circuit capacitor 550, which steadily charges frequency variation circuit capacitor 550 and increases the magnitude of frequency variation signal 400. The current that flows into frequency variation circuit capacitor 550 is derived from current source 525 because the current through transistor 590 is mirrored from transistor 580, which is mirrored from transistor 535.

During power up, when power-up signal 420 is low, the output of inverter 605 is high which turns on transistor 600 causing frequency variation signal 400 to go low. The frequency variation signal 400 is presently preferred to start from its lowest level to perform the soft start function during its first cycle of operation.

Steady-state operation of the pulse width modulated switch 262, i.e. non start up operation, will now be described. PWM oscillator 480 provides pulse width modulation oscillation signal 415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input provided at feedback terminal 295. When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input switch 435, thereby turning off switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 420, and maximum duty cycle signal 607. As long as each one of the signals is high, drive signal 610 is provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 420, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction.

Referring to Fig. 4, frequency variation signal 400 preferably has a period, which is greater than that of pulse width modulated oscillation signal 415. The presently preferred period for frequency variation signal 400 is twenty (20) milliseconds, in order to allow for a smooth start up period which is sufficiently longer than the period of pulse width modulated signal 415 which is presently preferred to be ten (10) microseconds. Drive signal 610 will be provided only when the magnitude of pulse width modulated signal 415 is less than the magnitude of frequency

variation signal 400. Further, frequency variation signal 400 will be preferably initiated starting from low voltage when power up signal 420 is provided.

Referring to Fig. 5, frequency variation signal 400 which is presently preferred to have a constant period is provided to the main oscillator 465. The magnitude of the pulse width modulator current 615 will approximately be the magnitude of frequency variation signal 400 divided by the resistance of resistor 510 plus the magnitude of the current produced by current source 470. In this way the pulse width modulator current 615 will vary with the magnitude of the frequency variation signal 400. The result is that the frequency of pulse width modulation signal is varied according to the magnitude of this current. It is presently preferred that the pulse width modulator current source produces a constant current having a magnitude of twelve point one (12.1) microamperes, and that frequency variation signal induced current 627 varies between zero (0) and eight hundred (800) nanoamperes. Thereby spreading the frequency of operation of the pulse width modulation oscillator 480 and reducing the average magnitude and the quasi-peak magnitude at all frequency levels of the EMI generated by the power supply.

Referring to Fig. 6, an alternate presently preferred pulse width modulated switch 262 includes all of the same components as described with respect to Fig. 3. In addition to these components, a second frequency variation circuit current source 660 and transistor 655 are added to the frequency variation circuit 405. Transistor 655 is activated only when the output of soft start latch 450 goes low. When transistor 655 is activated the current provided to the frequency variation circuit 405 increases as does the frequency of frequency variation signal 400. However, transistor 655 will only be turned on when the output of soft start latch 450 goes low, i.e. when the magnitude of frequency variation signal 400 first reaches the upper threshold after power up. The period of frequency variation signal 400 will then increase after its first half

cycle. This will decreases the period of the cycle during which the frequency is spread, without decreasing the frequency range. The benefit of the decreased cycle period will further decrease the quasi-peak levels of the EMI due to spending less time at each frequency level.

Referring to Fig. 7, operation of the frequency variation circuit 405 of Fig. 6 is depicted. Frequency variation signal 406 will preferably have a period of ten (10) milliseconds for its first half cycle. After that, when the transistor 655 is turned on the period is preferably decreased to five (5) milliseconds. Pulse width modulated switch 262 is presently preferred to be a monolithic device.

Referring to Fig. 8, a power supply comprises a bridge rectifier 710 that rectifies an input AC mains voltage. Power supply capacitors 720 charge with the rectified AC mains voltage to maintain an input DC voltage 725. A presently preferred range for input DC voltage 725 is approximately one hundred (100) to four hundred (400) volts to allow for operation based upon worldwide AC mains voltages which range between eighty five (85) and two hundred sixty five (265) volts. The presently preferred power supply also includes harmonic filter components 910 which in combination with capacitors 720 reduce the harmonic current injected back into the power grid. Transformer 730 includes a primary winding 740 magnetically coupled to secondary winding 750. The secondary winding 750 is coupled to a diode 760 that is designed to prevent current flow in the secondary winding 750 when the regulation circuit 850 is conducting (on-state). A capacitor 770 is coupled to the diode 760 in order to maintain a continuous voltage on a load 780 which has a feedback circuit coupled to it. A presently preferred feedback circuit comprises an optocoupler 800 and zener diode 820. The output of optocoupler 800 is coupled to the feedback terminal 825 of regulation circuit 850. The presently preferred regulation circuit 850 switches on and off at a duty cycle that is constant at a given input DC voltage ~~740~~ 725. A

regulation circuit power supply bypass capacitor 860 is coupled to and supplies power to regulation circuit 850 when the regulation circuit 850 is in the on-state.

Operation of the power supply will now be described. An AC mains voltage is input through EMI filter 700 into bridge rectifier 710 which provides a rectified signal to power supply capacitors 720 that provide input DC voltage 725 to primary winding 740. Regulation circuit 850, which preferably operates at a constant frequency and about constant duty cycle at a given input DC voltage 725, allows current to flow through primary winding 740 during its on state of each switching cycle and acts as open circuit in its off state. When current flows through primary winding 740 transformer 730 is storing energy, when no current is flowing through primary winding 740 any energy stored in transformer 730 is delivered to secondary winding 750. Secondary winding 750 then provides the energy to capacitor 770. Capacitor 770 delivers power to the load 780. The voltage across the load 780 will vary depending on the amount of energy stored in the transformer 730 in each switching cycle which is in turn dependent on the length of time current is flowing through primary winding 740 in each switching cycle which is presently preferred to be constant at a given input DC voltage 725. The presently preferred regulation circuit 850 allows the voltage delivered to the load to be maintained at a constant level.

It is presently preferred that the sum of the voltage drop across optocoupler 800 and the reverse break down voltage of zener diode 820 is approximately equal to the desired threshold level. When the voltage across the load 780 reaches the threshold level, current begins to flow through the optocoupler 800 and zener diode 820 that in turn is used to disable the regulation circuit 850. Whenever regulation circuit 850 is in the off-state the regulation circuit power supply bypass capacitor 860 is charged to the operating supply voltage, which is presently

preferred to be five point seven (5.7) volts by allowing a small current to flow from bypass terminal 865 to the regulation circuit power supply bypass capacitor 860. Regulation circuit power supply bypass capacitor 860 is used to supply power to operate regulation circuit 850 when it is in the on-state.

When the regulation circuit 850 is disabled, an open circuit condition is created in primary winding 740 and transformer 730 does not store energy. The energy stored in the transformer 730 from the last cycle of regulation circuit 850 is then delivered to secondary winding 750 which in turn supplies power to the load 780. Once the remaining energy in transformer 750 is delivered to the load 780 the voltage of the load 780 will decrease. When the voltage at the load 780 decreases below the threshold level, current ceases to flow through optocoupler 800 and regulation circuit 850 resumes operation either instantaneously or nearly instantaneously.

The presently preferred regulation circuit 850 has a current limit feature. The current limit turns off the regulation circuit 850, when the current flowing through the regulation circuit 850 rises above a current threshold level. In this way regulation circuit 850 can react quickly to changes such as AC ripple that occur in the rectified AC mains voltage, and prevents the propagation of the voltage changes to the load. The current limit increases the responsiveness of the regulation circuit to input voltage changes and delivers constant power output independent ~~for~~ the AC mains input voltage.

Although the presently preferred power supply of Fig. 8 utilizes current mode regulation and a feedback circuit that includes an optocoupler and zener diode, the present invention is not to be construed as to be limited to such a feedback method or circuit. Either current or voltage mode regulation may be utilized by the present invention without departing from the spirit and

scope of the present invention so long as a signal indicative of the power supplied to the load is supplied to the feedback terminal 825 of the regulation circuit 850. Additionally, although the presently preferred power supplies both utilize an optocoupler and zener diode as part of feedback circuits other feedback circuits may be utilized by the present invention without departing from the spirit and scope of the present invention.

Regulation circuit 850 also may have integrated soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of regulation circuit 850. A power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, regulation circuit 850 operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, regulation circuit 850 may also have frequency jitter functionality. That is, the switching frequency of the regulation circuit 850 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of Fig. 1 in that the frequency range of the presently regulation circuit 850 is known and fixed, and is not subject to the line voltage or load magnitude variations.

Referring to Fig. 9, frequency variation circuit 405 and main oscillator 465 function as described with respect to Fig. 3. In operation it is the variance of the high and low states of maximum duty cycle signal 607 that generates the frequency jitter functionality of the regulation circuit 850. A presently preferred regulation circuit 850 and its steady-state operation is depicted and described in copending patent application serial No. 09/032,520 which is hereby incorporated by reference in its entirety.

The regulation circuit of Fig. 9 can be modified to include a second current source to further increase the period of main oscillation signal 415 which achieves the same result and function as described with respect of Figs. 6 and 7.

The soft start functionality of the presently preferred regulation circuit 850 of Fig. 9, will shorten the on-time of switch 435 to less than the time of the maximum duty cycle signal 607 as long as the soft start enable signal 421 is provided and the magnitude of frequency variation signal 400 is less than the magnitude of main oscillation signal 415.

The presently preferred regulation circuit 850 preferably comprises a monolithic device.

While the embodiments, applications and advantages of the present invention have been depicted and described, there are many more embodiments, applications and advantages possible without deviating from the spirit of the inventive concepts described herein. Thus, the inventions are not to be restricted to the preferred embodiments, specification or drawings. The protection to be afforded this patent should therefore only be restricted in accordance with the spirit and intended scope of the following claims.

CLAIMS

What Is Claimed Is:

1. A pulse width modulated switch comprising:

a first terminal;

a second terminal;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

a frequency variation circuit that provides a frequency variation signal;

an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and

a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and a magnitude of said oscillation signal is below a variable threshold level.

2. The pulse width modulated switch of claim 1 wherein said first terminal, said second terminal, said switch, said oscillator, said frequency variation circuit and said drive circuit comprise a monolithic device.

3. The pulse width modulated switch of claim 1 wherein said frequency variation circuit comprises an additional oscillator that provides said frequency variation signal to said

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oscillator, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal.

4. The pulse width modulated switch of claim 1 further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

5. The pulse width modulated switch of claim 4 wherein said additional oscillator provides a soft start signal, and wherein said soft start circuit ceases operation when said soft start signal is removed.

6. The pulse width modulated circuit of claim 5 wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

7. The pulse width modulated switch of claim 1 wherein said frequency of said oscillation signal varies within said frequency range with a magnitude of said frequency variation signal.

8. The pulse width modulated switch of claim 1 wherein said oscillator comprises a an input that receives said frequency variation signal and a current source, wherein said frequency of said oscillation signal is a function of a sum of a magnitude of a current provided by said current source and a magnitude of said frequency variation signal.

9. The pulse width modulated switch of claim 1 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal and provides a substantially DC signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

10. The pulse width modulated switch of claim 1 wherein said variable threshold level is a function of a feedback signal received at a feedback terminal of said pulse width modulated switch.

11. A pulse width modulated switch comprising

a first terminal;

a second terminal;

a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;

a drive circuit that provides said drive signal according to said maximum duty cycle signal; and

a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.

12. The pulse width modulated switch of claim 11 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.

13. The pulse width modulated switch of claim 11 further comprising an additional oscillator that provides a soft start signal to said soft start circuit, and wherein when said soft start signal is removed said soft start circuit ceasing operation.

14. The pulse width modulated circuit of claim 13 wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation oscillation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

15. The pulse width modulated switch of claim 11 further comprising a frequency variation circuit that provides a frequency variation signal, wherein said oscillator provides an oscillation signal and wherein said soft start circuit provides said signal instructing said drive circuit to disable said drive signal when a magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

16. The pulse width modulated switch of claim 15 wherein said oscillator comprises an input that receives said frequency signal and said oscillation signal comprises a frequency range, and wherein said frequency of said oscillation signal varies within said frequency range according to a magnitude of said frequency variation signal.

17. The pulse width modulated switch of claim 16 wherein said oscillator further comprises a current source, wherein said frequency of said oscillation signal is a function of a sum of a magnitude of a current provided by said current source and said magnitude of said frequency variation signal.

18. The pulse width modulated switch of claim 11 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;

a power supply capacitor that receives said rectified signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

19. A regulation circuit comprising

a first terminal;

a second terminal;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

a drive circuit that provides said drive signal for a maximum time period of a cycle; and

a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.

20. The regulation circuit of claim 19 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.

21. The regulation circuit of claim 20 further comprising a frequency variation circuit that provides a frequency variation signal, wherein said oscillator provides an oscillation signal and wherein said soft start circuit provides said signal instructing said drive circuit to disable said drive signal when a magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

22. The regulation circuit of claim 19 further comprising an additional oscillator that provides a soft start signal to said soft start circuit, and wherein when said soft start signal is removed said soft start circuit ceasing operation.

23. The regulation circuit of claim 22 wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said additional oscillation signal, and

an inverter that receives said comparator signal and provides said soft start signal

24. The regulation circuit of claim 19 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.

25. The regulation circuit of claim 19 further comprising a feedback terminal and wherein when a signal is received at said feedback terminal said drive signal is discontinued for at least one cycle.

26. The regulation circuit of claim 19 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.

27. The regulation circuit of claim 26 further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level.

28. The regulation circuit of claim 19 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;

a power supply capacitor that receives said rectified signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

29. A regulation circuit comprising:

a first terminal;

a second terminal;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input; and

a frequency variation circuit that provides a frequency variation signal;

a drive circuit that provides said drive signal for a maximum time period of a time duration cycle;

wherein said time duration of said cycle varies according to said frequency variation signal.

30. The regulation circuit of claim 29 wherein said frequency variation circuit comprises an oscillator that provides said frequency variation signal.

31. The regulation circuit of claim 29 further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive according to a magnitude of said frequency variation signal.

32. The regulation circuit of claim 31 further wherein said frequency variation circuit provides a soft start signal, and wherein said soft start circuit ceases operation when said soft start signal is removed.

33. The regulation circuit of claim 32 wherein said frequency variation circuit further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

34. The regulation circuit of claim 29 wherein said first terminal, said second terminal, said switch, said frequency variation circuit, and said drive circuit comprise a monolithic device.

35. The regulation circuit of claim 29 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal and provides a substantially DC signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

36. The regulation circuit of claim 29 further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level.

37. The regulation circuit of claim 29 further comprising a feedback terminal and wherein when a signal is received at said feedback terminal said drive signal is discontinued for at least one cycle.

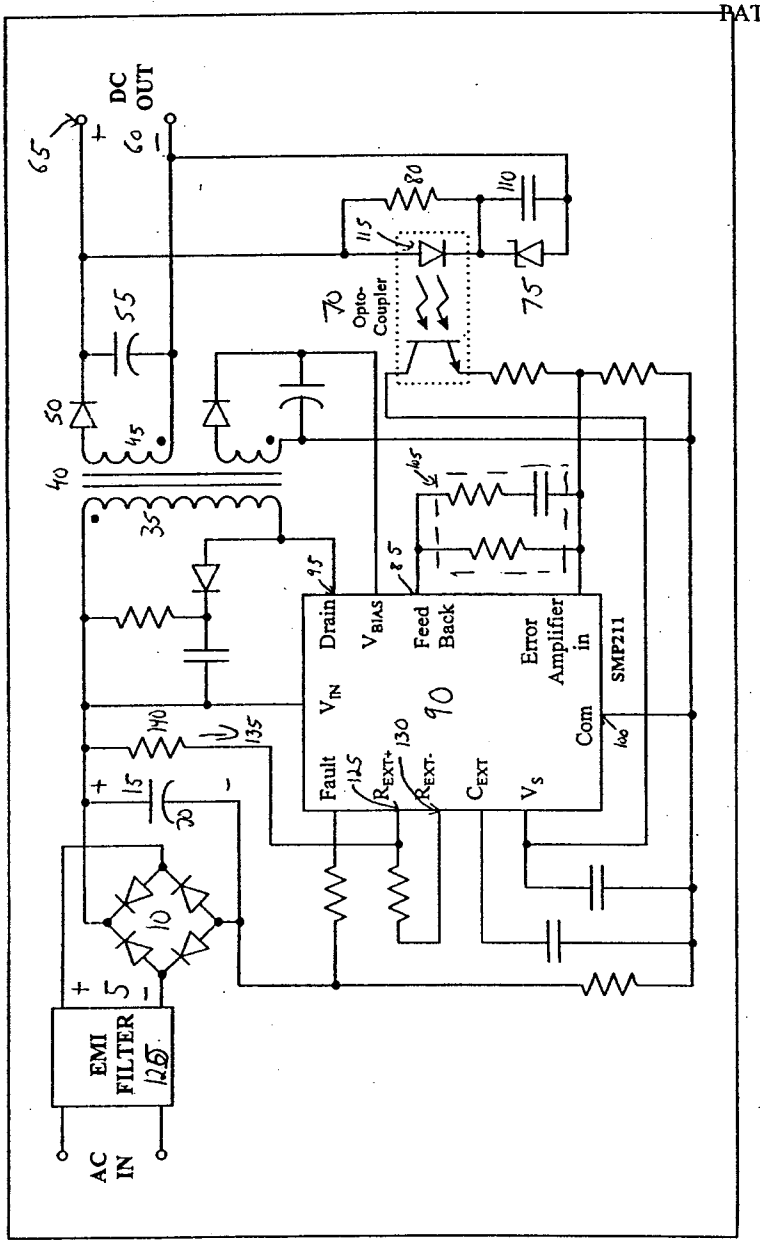

FIG. 1

Fig 9

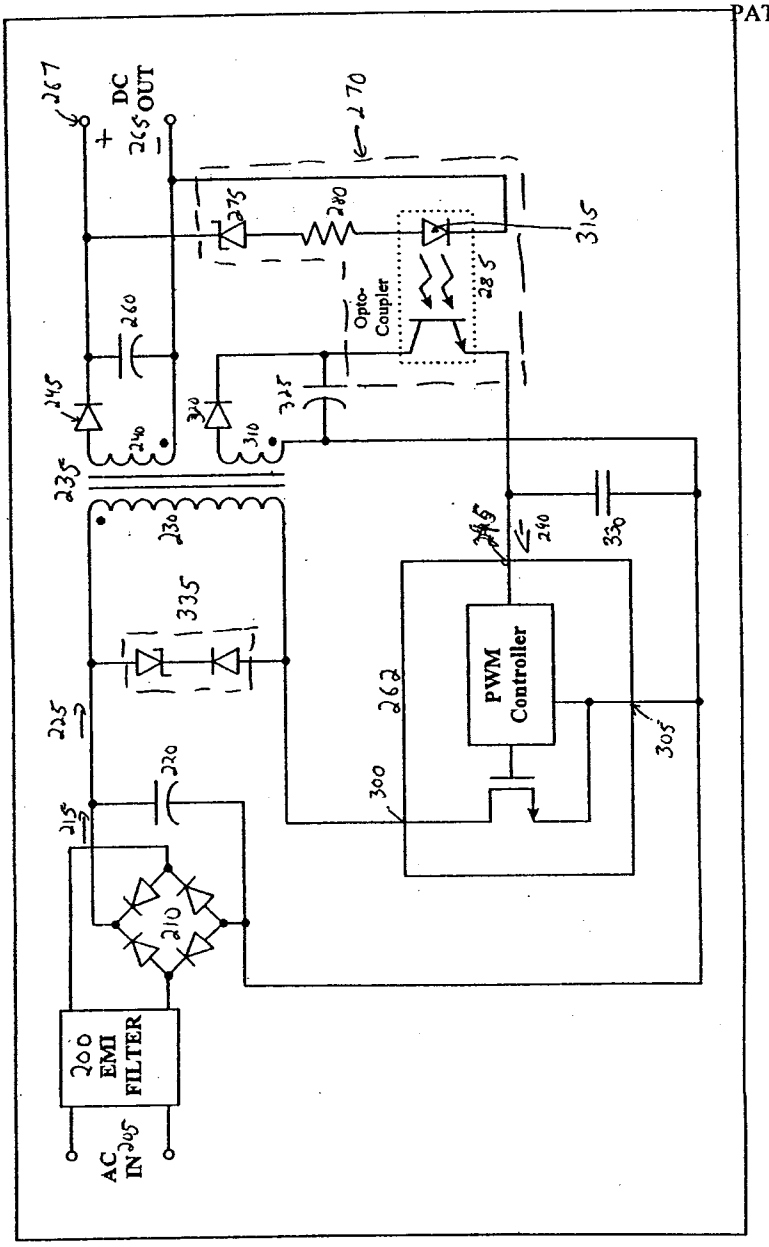

FIG. 2

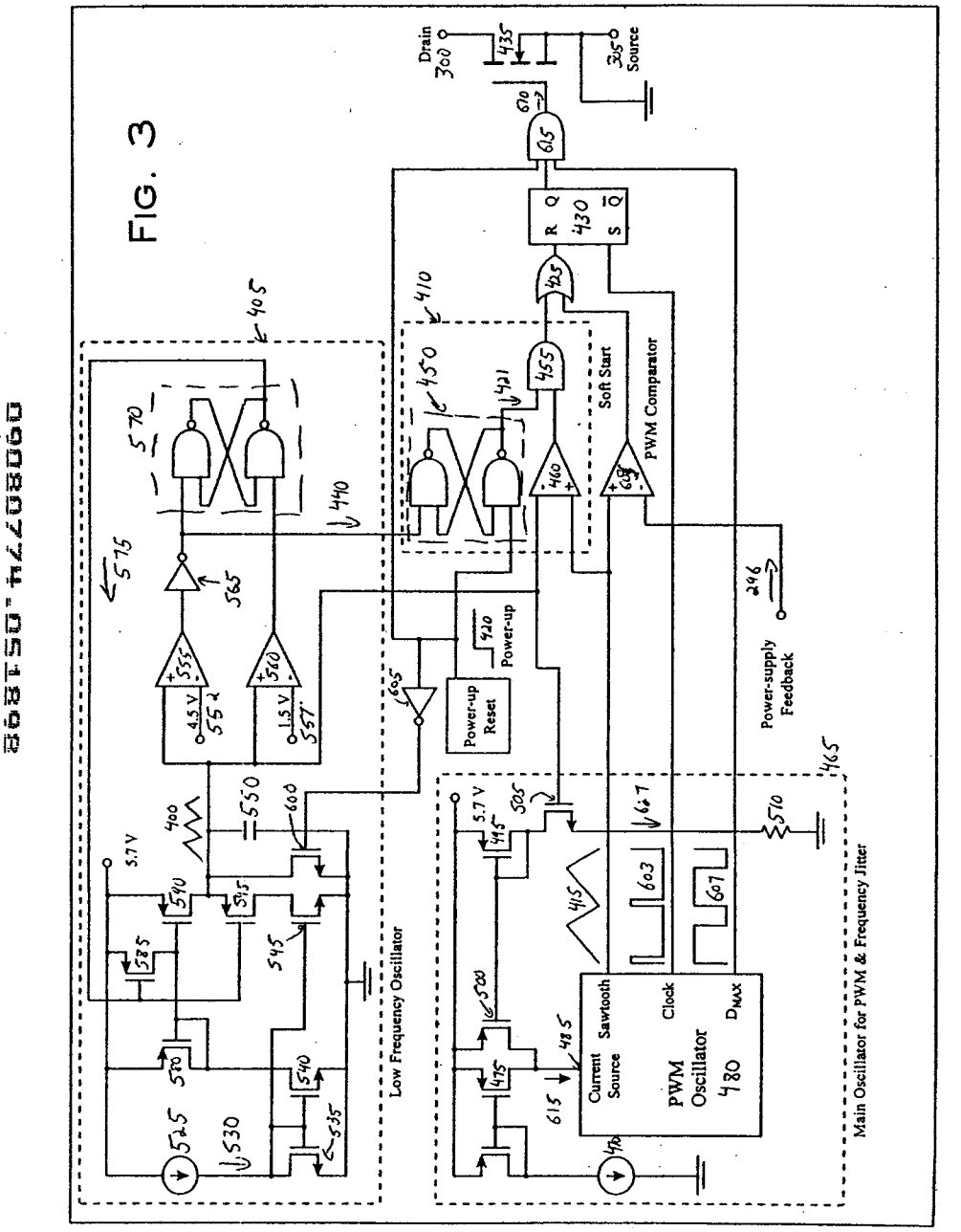

FIG. 3

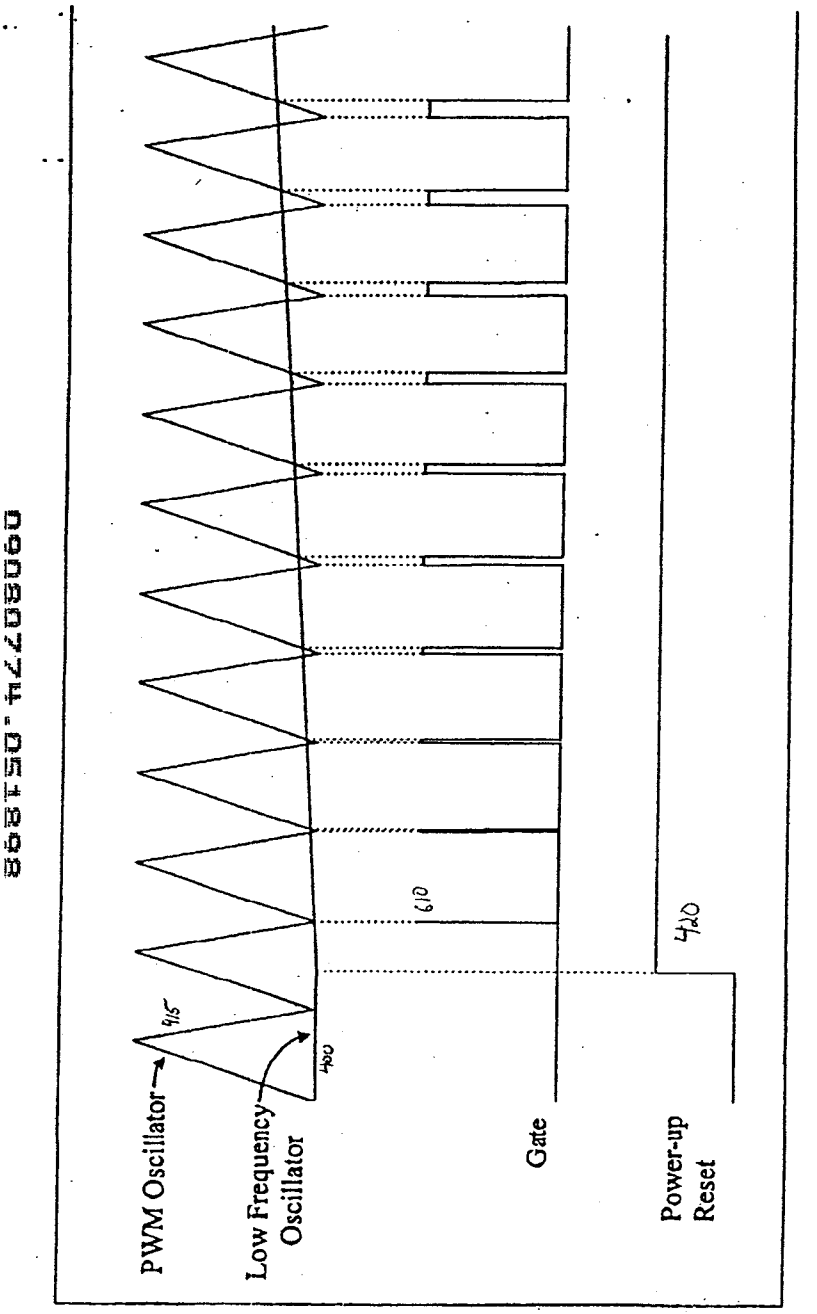

FIG. 4

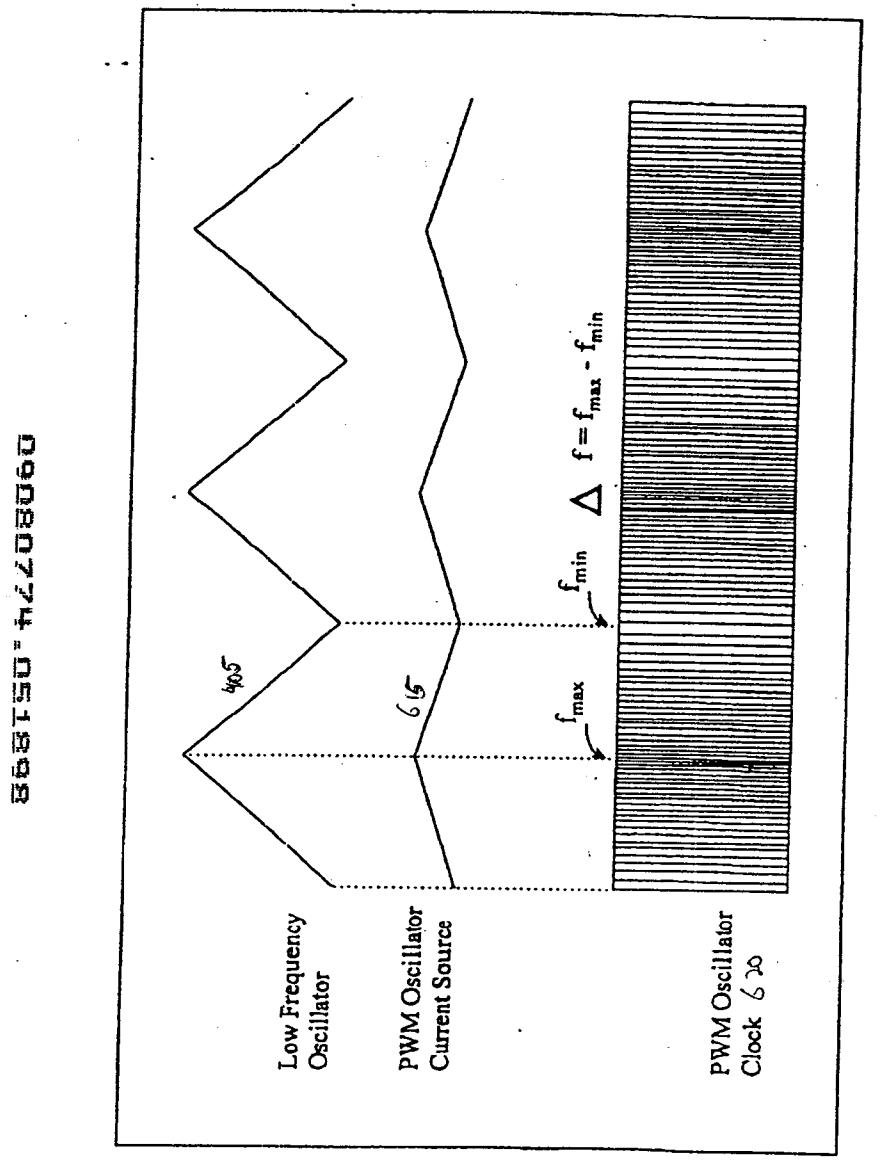

FIG. 5

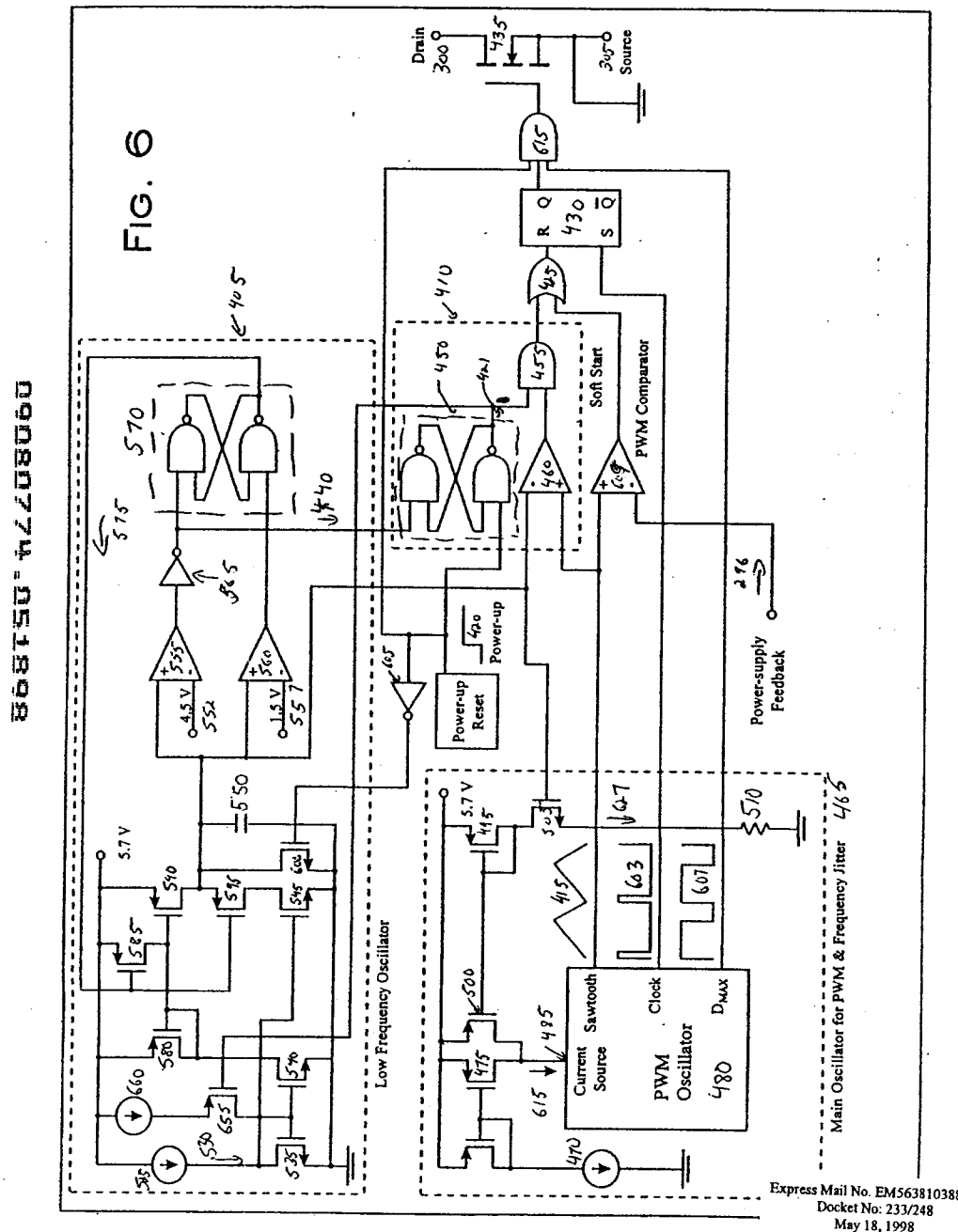

FIG. 6

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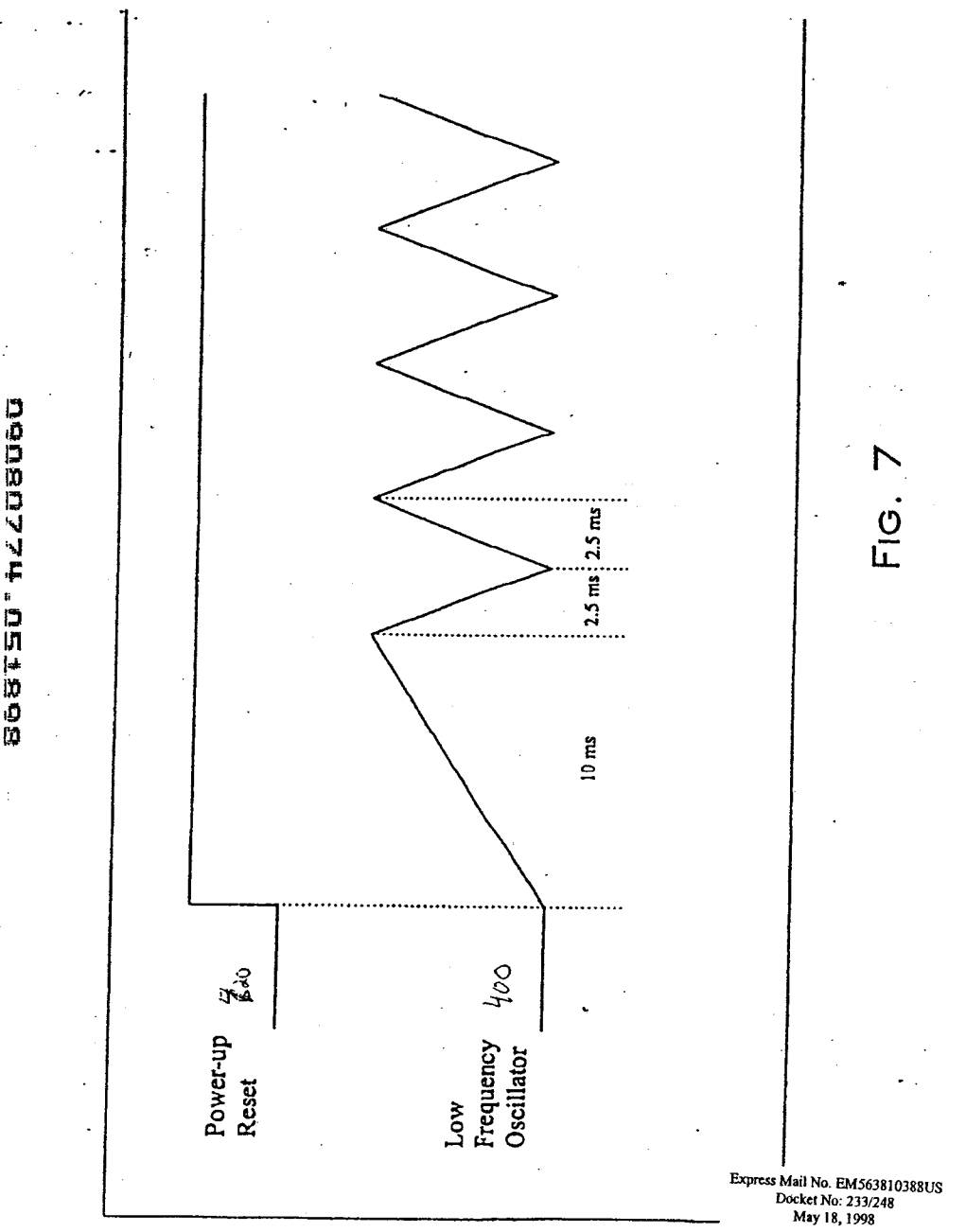

FIG. 7

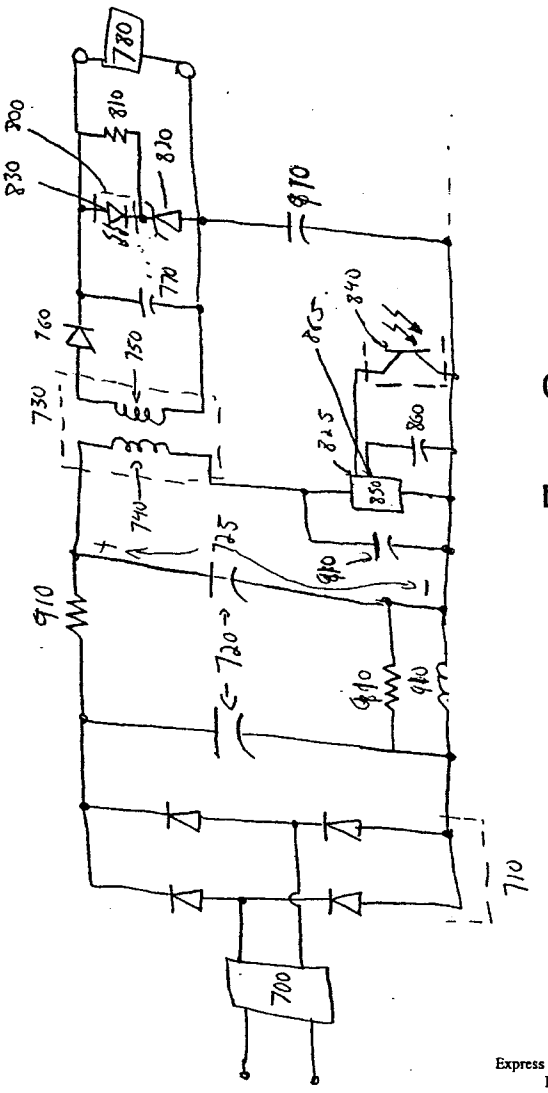

FIG. 8

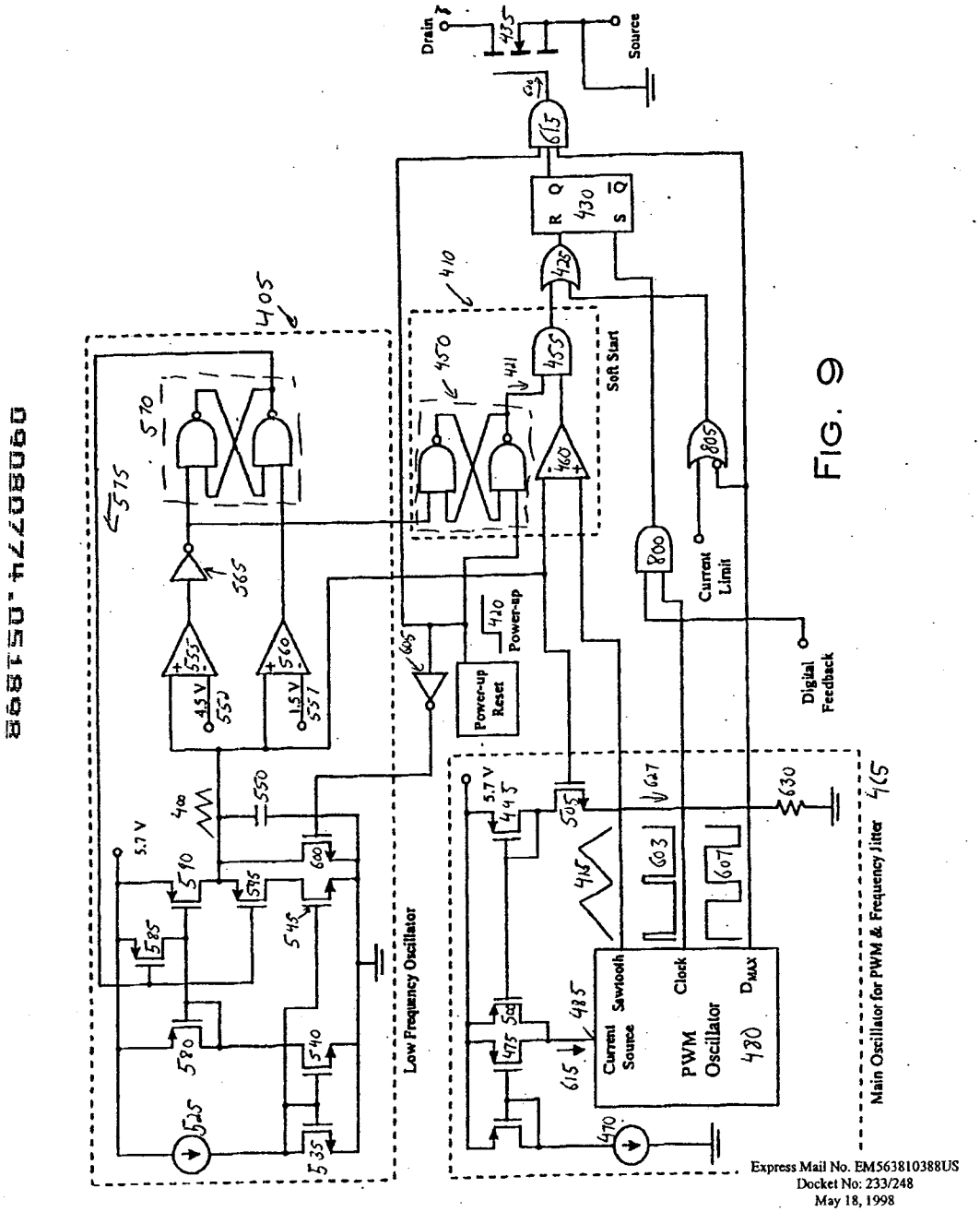

FIG. 9

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ABSTRACT

A pulse width modulated switch comprises a first terminal, a second terminal, and a switch that allows a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at a control input. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency of that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated switch further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

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May 18, 1998

DECLARATION
AND POWER OF ATTORNEY
Utility Application

LYON & LYON LLP

233/248

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "OFF-LINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER", the specification of which

Check One

☒ is attached hereto.
☐ was filed on _____ as Application Serial No.
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, ∋ 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, ∋ 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Application Number	Country	Date of Filing	Priority Claimed Yes%	Priority Claimed No%

I hereby claim the benefit under Title 35, United States Code, ∋ 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, ∋ 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, ∋ 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

Application Number	Date of Filing	Status–Patented, Pending or Abandoned

POWER OF ATTORNEY: As a named inventor, I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Roland N. Smoot, Reg. No. 18,718; Conrad R. Solum, Jr., Reg. No. 20,467; James W. Geriak, Reg. No. 20,233; Robert M. Taylor, Jr., Reg. No. 19,848; Samuel B. Stone, Reg. No. 19,297; Douglas E. Olson, Reg. No. 22,798; Robert E. Lyon, Reg. No. 24,171; Robert C. Weiss, Reg. No. 24,939; Richard E. Lyon, Jr., Reg. No. 26,300; John D. McConaghy, Reg. No. 26,773; William C. Steffin, Reg. No. 26,811; Coe A. Bloomberg, Reg. No. 26,605; J. Donald McCarthy, Reg. No. 25,119; John M. Benassi, Reg. No. 27,483; James H. Shalek, Reg. No. 29,749; Allan W. Jansen, Reg. No. 29,395; Robert W. Dickerson, Reg. No. 29,914; Roy L. Anderson, Reg. No. 30,240; David B. Murphy, Reg. No. 31,125; James C. Brooks, Reg. No. 29,898; Jeffrey M. Olson, Reg. No. 30,790; Steven D. Hemminger, Reg. No. 30,755; Jerrold B. Reilly, Reg. No. 32,293; Paul H. Meier, Reg. No. 32,274; John A. Rafter, Jr., Reg. No. 31,653; Kenneth H. Ohriner, Reg. No. 31,646; Mary S. Consalvi, Reg. No. 32,212; Lois M. Kwasigroch, Reg. No. 35,579; Lawrence R. LaPorte, Reg. No. 38,948; Robert C. Laurenson, Reg. No. 34,206; Carol A. Schneider, Reg. No. 34,923; Hope E. Melville, Reg. No. 34,874; Michael J. Wise, Reg. No. 34,047; Richard J. Warburg, Reg. No. 32,327; David T. Burse, Reg. No. 37,104; Jeffrey A. Miller, Reg. No.35,287; Bernard F. Rose, Reg. No. P-42,112; Michael J. Bolan, Reg. No. P-42,339; Lynn Y. McKernan, Reg. No. P-41,986; and Dmitry R. Milikovsky, Reg. No. P-41,999.

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Update 4/97

APPLICABLE STATUTES & RULES

37 CFR 1.56 DUTY TO DISCLOSE INFORMATION MATERIAL TO PATENTABILITY.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by ss 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in;

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

35 U.S.C. 102. CONDITIONS FOR PATENTABILITY; NOVELTY AND LOSS OF RIGHT TO PATENT

A person shall be entitled to a patent unless–

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States, or

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent, or

(f) he did not himself invent the subject matter sought to be patented, or

(g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

35 U.S.C. 103. CONDITIONS FOR PATENTABILITY; NON-OBVIOUS SUBJECT MATTER

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

35 U.S.C. 119. BENEFIT OF EARLIER FILING DATE IN FOREIGN COUNTY; RIGHT OF PRIORITY (Applicable Portion)

An application for patent for an invention filed in this country by any person who has, or whose legal representatives or assigns have, previously regularly filed an application for a patent for the same invention in a foreign county which affords similar privileges in the case of applications filed in the United States or to citizens of the United States, shall have the same effect as the same application would have if filed in this county on the date on which the application for patent for the same invention was first filed in such foreign county, if the application in this county is filed within twelve months from the earliest date on which such foreign application was filed; but no patent shall be granted on any application for a patent for an invention which has been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country, or which had been in public use or on sale in this country more than one year prior to such filing.

35 U.S.C. 120. BENEFIT OF EARLIER FILING DATE IN THE UNITED STATES

An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, by the same invention shall have the same effect, as to such invention, as though filed on the date of the prior application, if filed before the patenting or abandonment of or termination of proceedings on the first application or on an application similarly entitled to the benefit of the filing date of the first application and if it contains or is amended to contain a specific reference to the earlier filed application.

35 U.S.C. 112. SPECIFICATION (Applicable Portion)

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enabler any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification shall conclude with one or more claims particularly pointing out and distinctive claiming the subject matter which the applicant regards as his invention.

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203	FULL NAME OF INVENTOR	FIRST Name Leif	Middle Initial(s)	LAST Name Lund		
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204	FULL NAME OF INVENTOR	FIRST Name	Middle Initial(s)	LAST Name		
	RESIDENCE & CITIZENSHIP	City	State or Foreign Country	County of Citizenship		
	POST OFFICE ADDRESS	Post Office Address	City	State or Country	Zip Code	

09080774 . 05138998

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 201 Balu Balakirshnan
Date 5-14-98

Signature of Inventor 202 Alex Djenguerian
Date 5/14/98

Signature of Inventor 203 Leif Lund
Date 05-14-98

(Signatures should conform to names as presented at 201 et seq. above.)

DPOA.Uti Update 4/97

POWER OF ATTORNEY

LYON & LYON LLP
DOCKET INFORMATION
233/248

Power Integrations, Inc., assignee(s) of the application for United States Letters Patent for a **"OFF-LINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER"**

by Balu Balakirshnan, Alex Djenguerian and Lief Lund
(Inventor)

☒ executed on even date herewith, or
having Serial No. _____ filed _____,

a copy of the assignment of which is attached hereto, do(es) hereby appoint as attorneys of record with full power of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Roland N. Smoot, Reg. No. 18,718; Conrad R. Solum, Jr., Reg. No. 20,467; James W. Geriak, Reg. No. 20,233; Robert M. Taylor, Jr., Reg. No. 19,848; Samuel B. Stone, Reg. No. 19,297; Douglas E. Olson, Reg. No. 22,798; Robert E. Lyon, Reg. No. 24,171; Robert C. Weiss, Reg. No. 24,939; Richard E. Lyon, Jr., Reg. No. 26,300; John D. McConaghy, Reg. No. 26,773; William C. Steffin, Reg. No. 26,811; Coe A. Bloomberg, Reg. No. 26,605; J. Donald McCarthy, Reg. No. 25,119; John M. Benassi, Reg. No. 27,483; James H. Shalek, Reg. No. 29,749; Allan W. Jansen, Reg. No. 29,395; Robert W. Dickerson, Reg. No. 29,914; Roy L. Anderson, Reg. No. 30,240; David B. Murphy, Reg. No. 31,125; James C. Brooks, Reg. No. 29,898; Jeffrey M. Olson, Reg. No. 30,790; Steven D. Hemminger, Reg. No. 30,755; Jerrold B. Reilly, Reg. No. 32,293; Paul H. Meier, Reg. No. 32,274; John A. Rafter, Jr., Reg. No. 31,653; Kenneth H. Ohriner, Reg. No. 31,646; Mary S. Consalvi, Reg. No. 32,212; Lois M. Kwasigroch, Reg. No. 35,579; Lawrence R. LaPorte, Reg. No. 38,948; Robert C. Laurenson, Reg. No. 34,206; Carol A. Schneider, Reg. No. 34,923; Hope E. Melville, Reg. No. 34,874; Michael J. Wise, Reg. No. 34,047; Richard J. Warburg, Reg. No. 32,327; David T. Burse, Reg. No. 37,104; Jeffrey A. Miller, Reg. No. 35,287; Bernard F. Rose, Reg. No. P-42,112; Michael J. Bolan, Reg. No. P-42,339; Lynn Y. McKernan, Reg. No. P-41,986; and Dmitry R. Milikovsky, Reg. No. P-41,999.

Send Correspondence to:	LYON & LYON LLP First Interstate World Center 47th Floor, 633 W. Fifth St. Los Angeles, CA 90071-2066	Direct Telephone Calls to: Dmitry R. Milikovsky, Esq. (408) 993-1555

I, the undersigned, declare that I am the (an) assignee of the above-identified application or, if the assignee is a corporation, partnership or other association, I am authorized to make this appointment on behalf of the assignee and I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of Assignee	Power Integrations, Inc.	
Post Office Address	477 North Mathilda Avenue, Sunnyvale, California 94086	
Signature of Declarant or Assignee	Balu Balakirshnan	Date: May 14, 1998

Full Name of Declarant If Other Than Assignee	Balu Balakirshnan
Title of Declarant	Vice-President, Marketing and Engineering
Address of Declarant	13917 Albar Court, Saratoga, California 95070

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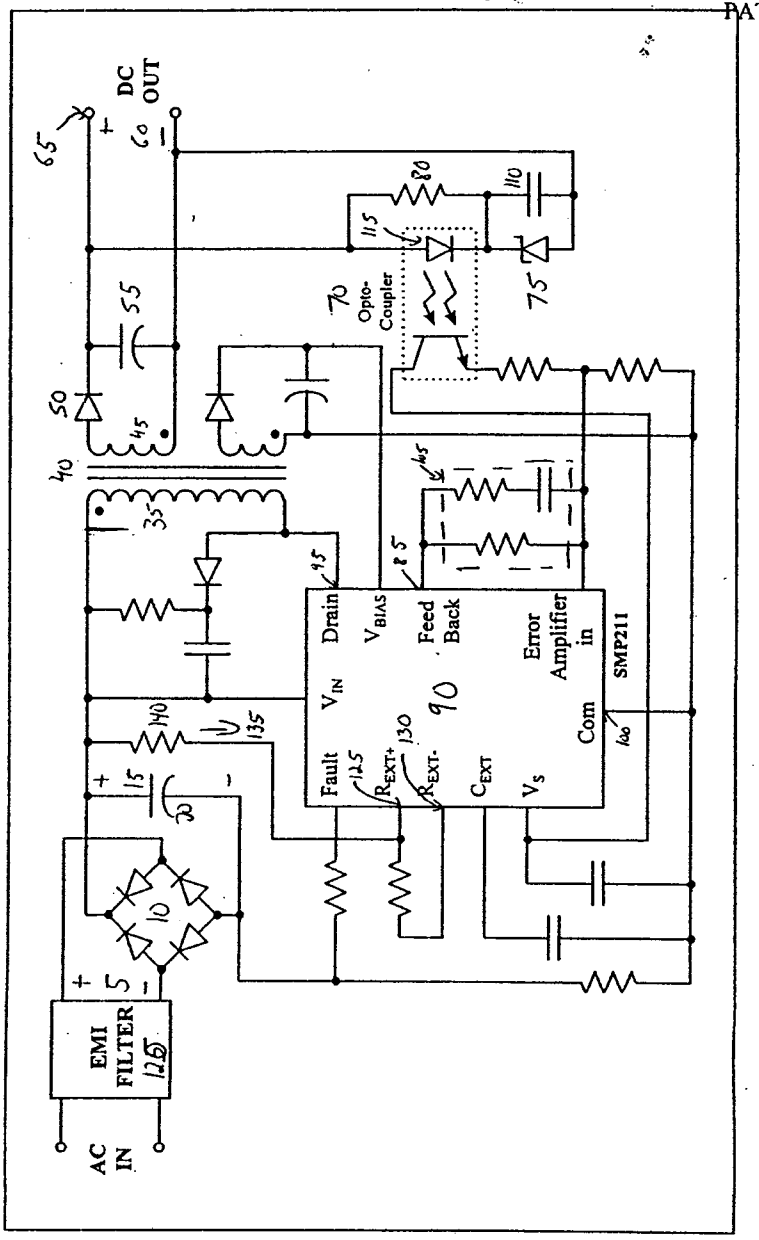

FIG. 1

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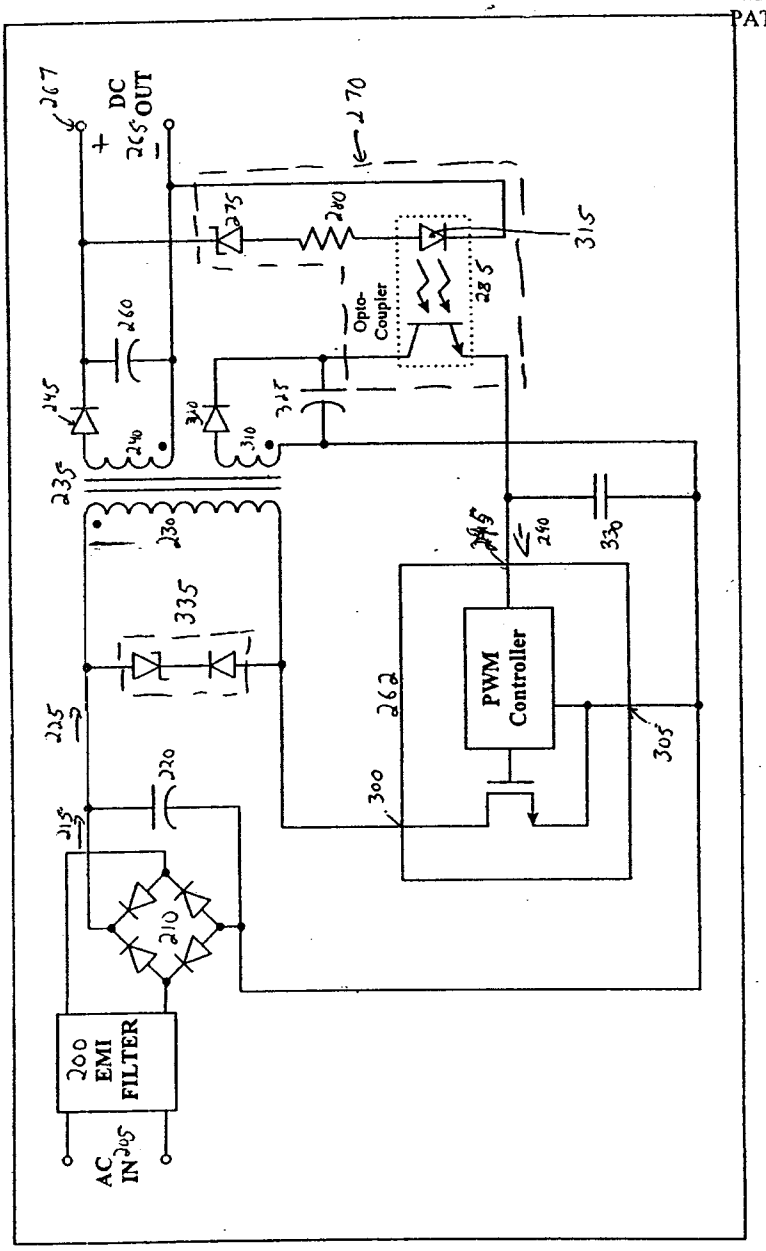
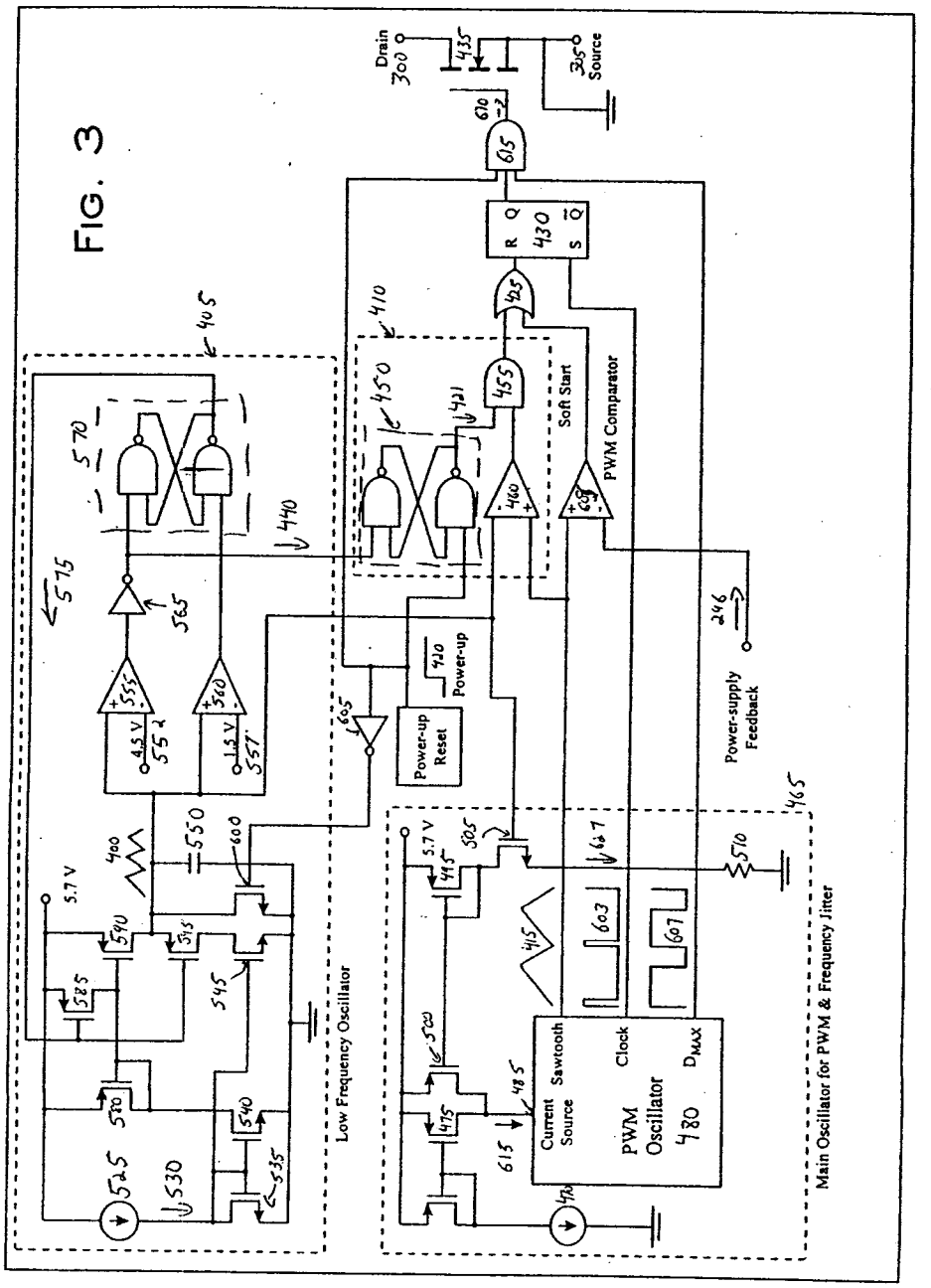


FIG. 2

FIG. 3



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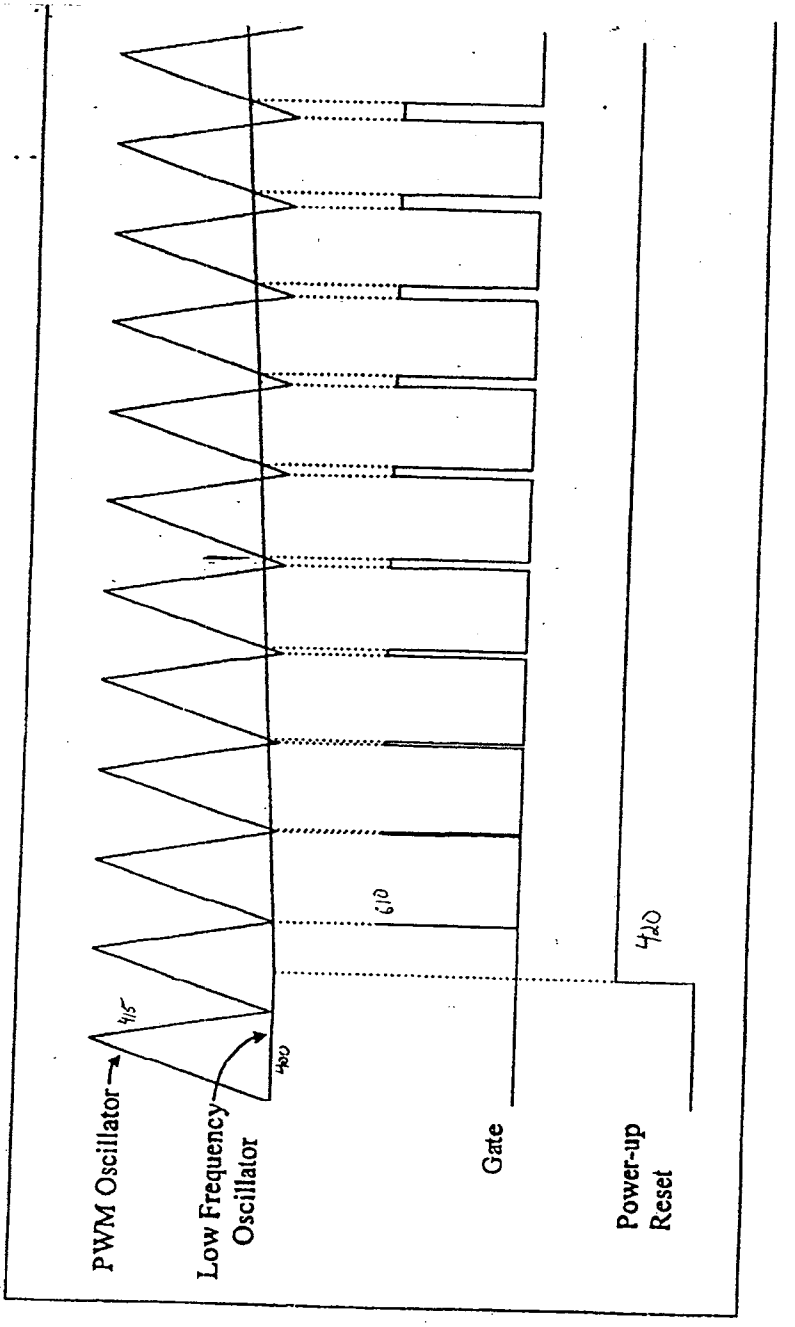

FIG. 4

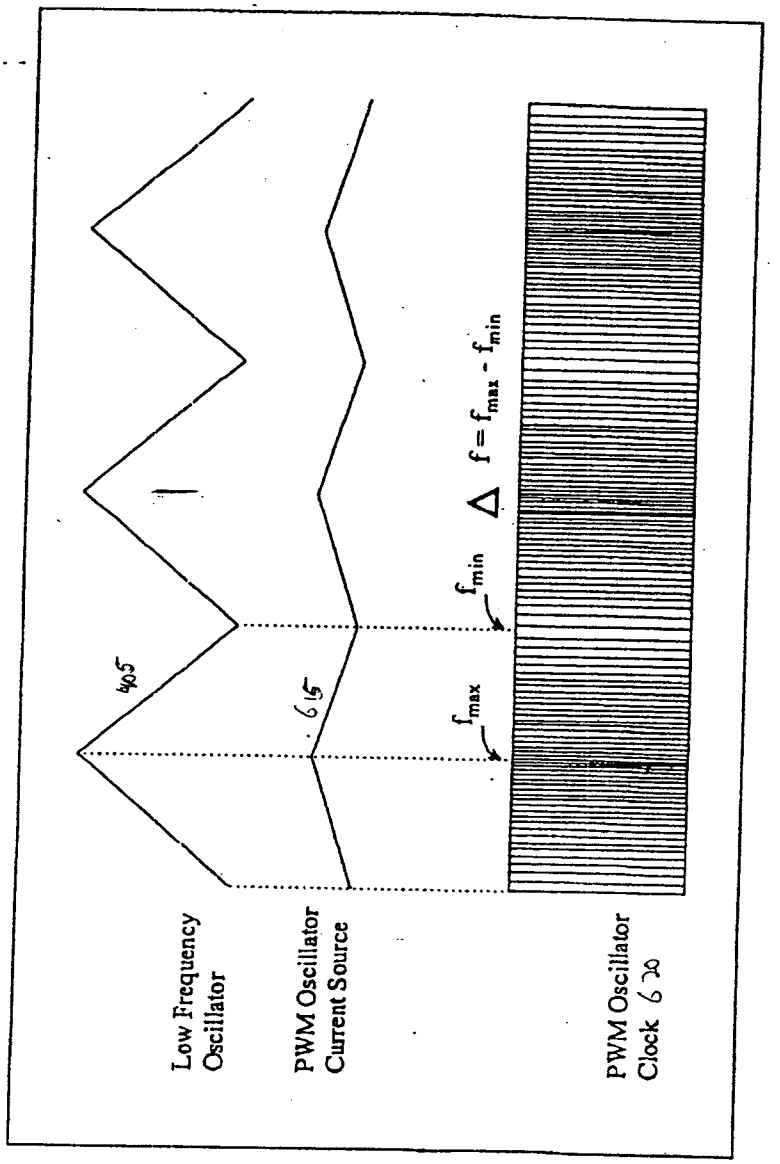

FIG. 5

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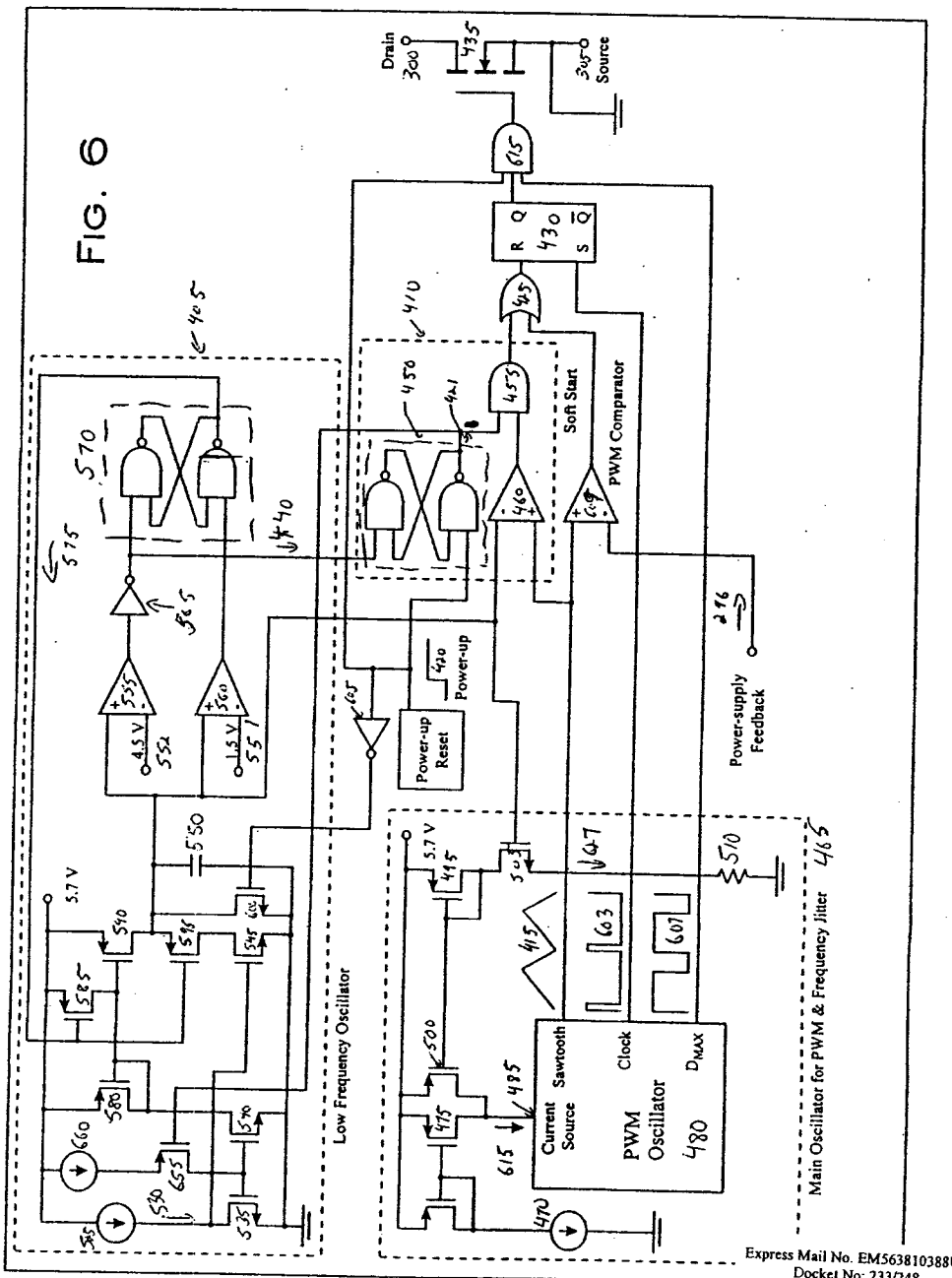
FIG. 6



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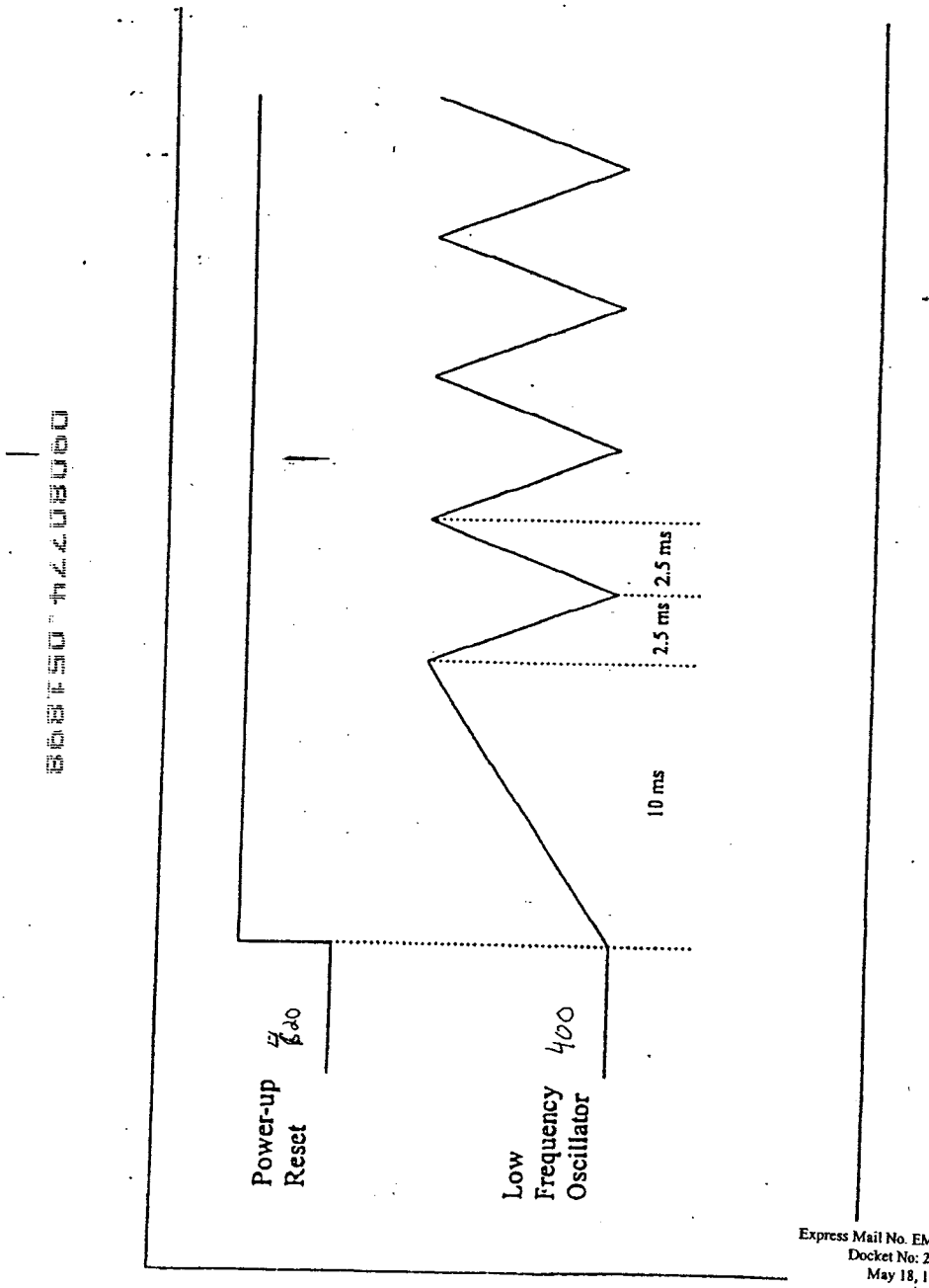

FIG. 7

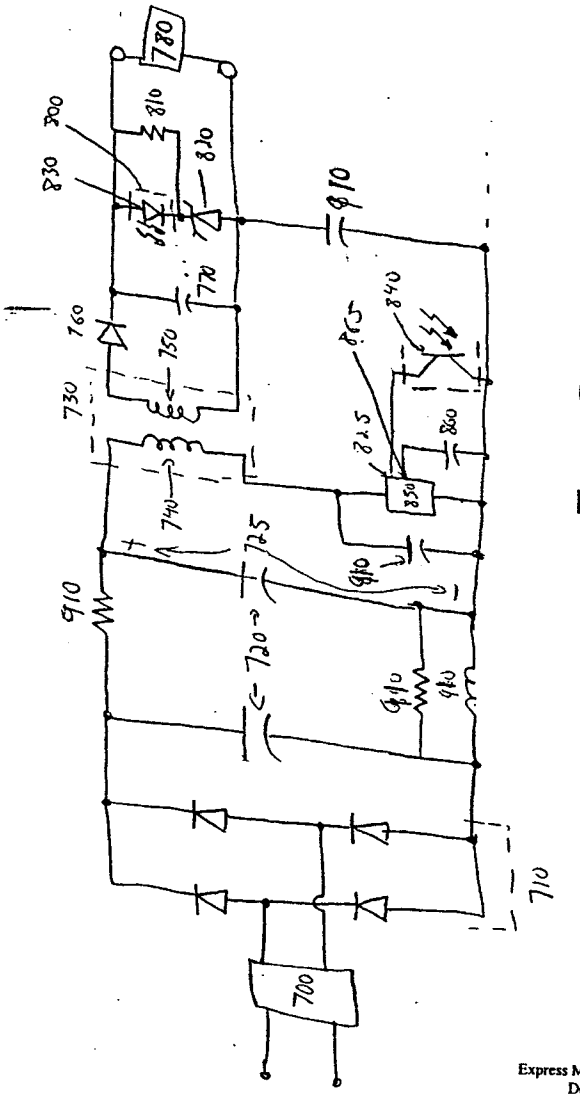

FIG. 8

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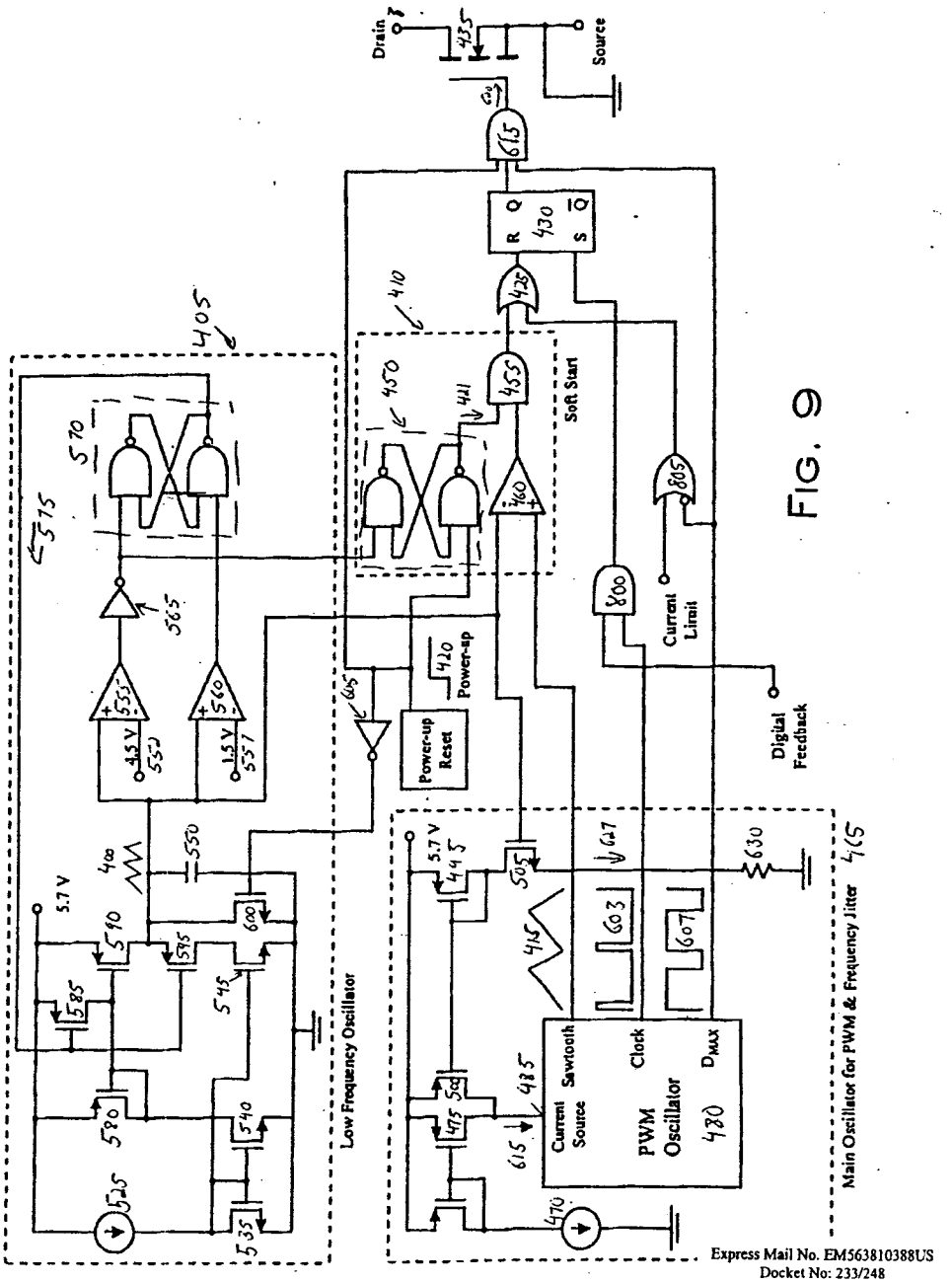

FIG. 9

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